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WARNING

Because of possible shock or fire hazards, connection of this instrument should be performed in compliance with the National Electrical Code (ANSI C1) and/or any other requirements which are applicable to the user.

Installation, operation, and maintenance should be performed only by qualified personnel.

TM-110532

VOLUME 2

SERVICE MANUAL

626-PA-6012

COMMUNICATIONS MODULE

31 October 1983

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DRANETZ

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626-PA-6012 COMMUNICATIONS MODULE

1 INTRODUCTION

This manual provides maintenance instructions for the 626-PA-6012 Communications Module Plug-in which is used in the Model 626 Universal Disturbance Analyzer. Included in this volume are the theory of operation, maintenance, and parts list for the 6012. For operating instructions, refer to Volume 1 of this manual.

2 THEORY OF OPERATION

2.1 Block Diagram Description

The 626-PA-6012 Communications Module is designed to provide mass storage for the data transmitted out of the RS232C port of the 626 mainframe, and to provide a bi-directional interface between the phone lines and the RS232C port of the mainframe, thus allowing remote operation. The 6012 also interfaces to the 626 as a normal plug-in. As a result of these requirements, the 6012 contains its own processor that, for the most part, runs independently of the 626's CPU. For the sake of clarity, the on-board processor will be referred to as either the 6012 CPU or CPU. The mainframe CPU will be referred to as the 626 CPU. The entire 6012 plug-in, which includes the modem board and the CPU/Interface board, is referred to as the 6012.

The 6012 is divided into three basic sections: (1) the communications interface/control; (2) the 626 interface; and (3) the modem. The communications interface/control section of the CPU/Interface Board includes the CPU, CMOS RAM, RS232C port, and modem control circuitry. The module interface circuitry, which permits the 6012 to communicate with the 626 mainframe as a normal module, is also on the CPU/Interface board. A second board contains the modem and phone line interface circuitry. This board is FCC-registered and, due to FCC regulations, may only be serviced by the manufacturer. Therefore, it will only be mentioned in the following, as it affects the operation of the CPU/Interface Board.

2.2 Detailed Circuit Description

2.2.1 CPU

The 6012 on-board processor is a 6502 micro-processor (U7) with an 8-bit data bus and a 16-bit address bus. The 1 MHz clock for the processor is derived from the ENA output (phase 2) of the 626 CPU. The ENA, R/W, MYW (not), and MYR (not) signals are generated from the on-board processor's Phase 2 clock and the R/W line by a group of inverters (U10) and OR gates (U38). The NMI and RDY lines are not used, thus they are tied high. The RESET line for the 6012's CPU is taken from the RESET line of the 626 CPU.

The upper half of the 64k addressable memory space ($8000-$FFFF) is divided into eight select lines, which are derived from the decoding of A12-A15 by a 3-8 decoder (U9). The functions of these select lines are defined in Table 1.

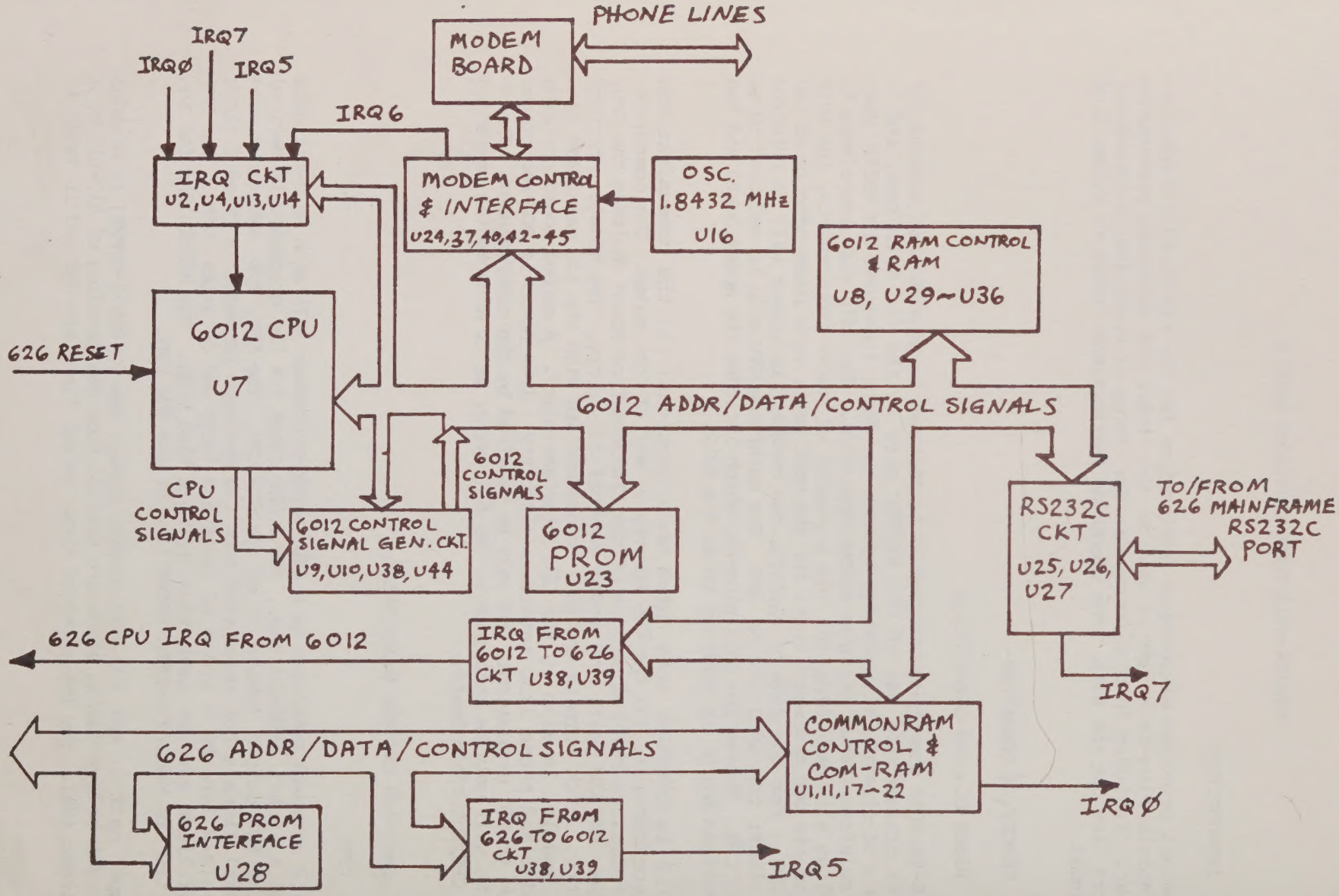

Figure 1. 6012, Block Diagram

Table 1
6012 CPU Select Lines

Signal	Function
BS8	read IRQ data
BS9	set and clear IRQ to/from module
BSA	modem control
BSB	common RAM control and data
BSC	ACIA of RS232C port
BSD	ACIA of modem control
BSE	dialer control
BSF	program ROM

The lower half of the address space ($0000-$3FFF) contains the processor and data stack RAM (U29-U36). These eight 2K x 8 CMOS RAM chips are enabled by eight RAM chip select lines, which are derived from the decoding of A11-A15 by 3-8 decoder U8. The MYW and MYR lines control the direction of the internal tri-state buffers of the CMOS RAM chips.

The CPU's 12-bit address bus (A0-A11) is formed from the processor's address lines and buffered by a pair of always enabled tri-state buffers (U5 and U6). The upper 4 address lines (A12-A15) of the processor are only used within the CPU. The eight bit bi-directional data bus passes through an 8-bit transceiver chip (U43), whose direction is controlled by the R/W line and is always enabled, except when the PROM (U2) is being accessed via BSF.

The CPU is responsible for controlling the CMOS RAM, RS232C port, and modem interface circuitry. In addition, it is responsible for controlling the direction of data flow during any and all internal exchanges and stores of data, and during external transmission and receipt of data to/from the phone lines or RS232C port.

All IRQs within the 6012 (IRQ0, IRQ1, IRQ6, and IRQ7) are gated through tri-state buffers (U2 and U3), and are accessed by the CPU via BS8. The four IRQ lines are AND'ed together by a single 4 input AND gate (U4) in order to provide a single IRQ line to the processor. The IRQ circuitry operates using negative logic, therefore a low state on any IRQ line results in an interrupt to the CPU.

2.2.2 RS232C PORT

The RS232C port of the 6012 is configured as a DTE to permit direct connection to the RS232C port of the 626 mainframe via Dranetz Interface Cable #110540. The port consists of a 6850 ACIA (U25) and a set of drivers and receivers (U27 and U26) which converts the 0-5 Vdc logic of the ACIA to/from +/- 12 Vdc as required by the RS232C port. Receiver Full or CTS and DSR control line state changes are signalled to the CPU via IRQ7. The ACIA is enabled by BSC, and the register selection is controlled by the internal decoding of A0, A6, A7, R/W and ENA. The baud rate clock of the 626 is used to generate the transmit/receive baud rate clock for the 6012's RS232C port. This insures that the 6012's ACIA is always synchronized to that of the 626's RS232C port,

regardless of its rate.

2.2.3 MODEM CONTROL

The modem is controlled primarily by a 6551 ACIA (U24). The ACIA provides and monitors the control and data lines of the modem and is enabled by BSC with the various registers being selected by decoding of A0, A1, A7, R/W, and ENA lines. IRQ6 is generated by changes in status of Xmit Reg Empty, DSR, DCD and/or CTS. The Test and Dial Enable control lines are supplied to the modem via a 4-bit latch (U37). A Tri-state buffer, U41, is used to monitor the following modem signals: Dial Tone, Ring, RTS, CTS, and RCV. Both the latch and buffer are enabled by BSA and the MYW and MYR lines, respectively. The baud rate clock is software programmable and derived from the oscillator circuit composed of a 1.8432 MHz crystal (Y1), an RC network (C13, R12, R13, and R14), and several inverters (U16).

The modem requires an externally supplied dialing pulse for the phone digits. The dialing pulses are generated by dialer chip U40. Driven by a 16 kHz clock (U45), it provides for a 61/39 % Make/Break ratio pulse for the modem when the Dial Enable line is active. The dialer chip can store a maximum of 16 digits. During power on or after the programming of a new phone number, the digits are latched into a 4-bit latch (U42), then strobed into the dialer chip with the dial enable line off. When a call out is requested, the dialer chip is told to redial the stored digits. When a wait-for-dial-tone digit is encountered, the Wait signal is turned on until a Dial Tone signal is detected. The various dialer control signals--Strobe, Wait, Call Request, and Redial--are held in 4-bit latch, U43.

2.2.4 MODULE INTERFACE

The module interface circuitry consists of a 4K x 8 PROM (U28) and buffers U2 and U3. PROM U28 contains the program that allows the 6012 to interface to the 626 mainframe as a normal module. One of the two available select lines is used to access the PROM and its buffer to the data bus lines. The buffer direction is controlled by the R/W line of the 626.

All changes in status and operating conditions of either the module or CPU are signalled to the other side via interrupts. A set of flip-flops (U39) is used for sending and receiving IRQs to/from the module or 6012 CPU. The 6012 CPU can send an IRQ to the module by accessing $9700. After servicing the IRQ, the module clears the interrupt by addressing $XC00, where X is either 1,3,5,7, or 9, depending on the channel number. The module software sends interrupts to the 6012 CPU by selecting $XA00, which in turn is cleared by the 6012 CPU by addressing $9B00. The 6012 CPU reads IRQ0 by enabling the buffer controlled by BS8. Table 3 summarizes the control signals used to set and clear interrupts between the CPU and the 626 module sections of the 6012.

Table 3
Interrupt Control Signals

Address	Function
$9700	6012 CPU sends IRQ to module
$9B00	6012 CPU clears IRQ from module
$XA00	module sends IRQ to 6012 CPU
$XC00	module clears IRQ from 6012 CPU

2.2.5 COMMON RAM

The remaining ciruitry on the CPU/Interface Board is for the Common RAM. This 1k x 4 RAM is used as a mailbox to pass data back and forth between the module software and the CPU software, signalling the presence of new data (or mail) by setting the appropriate IRQ, as mentioned above. The address and data lines of the RAM can be controlled by either side (or software), but not simultaneously. A request to control the RAM must first be made ($X000 or $B000, module or CPU, respectively). If the other side does not have control, there is a flip flop (U21) that will grant access and control of the chip. The request granted signal is Bit 7 of the data, which can always be read even without control. Each side has its own read and write buffers (U15 and U14, or U13 and U12, module or CPU). Reading is enabled by $X600 or $B600, while writing is enabled by $X400 or $B400. The address lines for the RAM come from the side which has control--from the 626 through buffer U20 (module) or from the 6012 CPU through buffer U19.

If one side already has control of the RAM, then any Request from the other side will be blocked by a NOR gate (U11) until the controlling side relinquishes its control. Control is relinquished by a Common RAM Reset signal ($X200 or $B200) which is the last of the four signals generated by decoding A9, A10, ENA and the BSX or BSB (module or CPU). Exact simultaneous requests are impossible since the 6012 CPU runs off the Phase 2 and not the Phase 1 clock of the 626 CPU, therefore skewing all actions by 500nsec. The Common RAM control signals are summarized in Table 4.

TABLE 4
COMMON RAM CONTROL SIGNALS

Address	Function
(module/CPU)	
$X000/$B000	request control of COM-RAM
$X200/$B200	relinquish control of COM-RAM
$X400/$B400	write to COM-RAM
$X600/$B600	read from COM-RAM

2.2.6 MODEM BOARD

The modem board is a 300 baud, full duplex modem. It has auto-answer and dial up capabilities, as well as a self-test mode, where the xmitter is looped back

to the receiver just before the switch hook. The control for the modem is provided by the afore-mentioned Modem Control Section of the CPU/Interface Board. The phone connections are brought out to the rear panel to a connector that will accept a standard RJ11C phone jack. Any servicing of the modem must be done by the manufacturer, as stated by the FCC Rule X, Part 68.

2.2.7 REAR PANEL

The double width rear panel contains a 25-pin female D connector, an RJ11C compatible phone connector, and a red LED. The red LED indicates when the phone line is active. The rear panel also contains vent holes due to the power consumed by the plug-in. The 6012 is placed preferably in Channel 1 and 2, so that the interface cable to the Communications port of the 626 is not intermixed with the input leads of the other modules, for noise reduction and safety reasons.

3 REPLACEABLE PARTS LIST

The replaceable parts list identifies the replaceable parts in the plug-in. The following is presented for each such part: reference designation (if applicable), part number, manufacturer's code number, and a description. Figure 2 identifies the parts printed on circuit board A1.

REPLACEABLE PARTS LIST

626-PA-6012

PC Board, Communications Module P/N 110532

REF DESIG	PART NO.	MAN CODE NO.	DESCRIPTION
C1-C5,C12, C14-C23,C28-40	103209-G2	23207	Cap, .22uF +/-20%, 50V
C6-C9	104022-G4	23207	Cap, 200pF +/-5%, 100V
C10,C24	103208-G4	23207	Cap, .1uF +/-20%, 50V
C11	104071-G2	23207	Cap, .022uF +/-5%, 400V
C13	104071-G1	23207	Cap, .047uF +/-5%, 250V
C25-C27	104055-G2	23207	Cap, 47uF +/-10%, 20V
R1-R4,R11	RCR07G103J		Res, 10K +/-5%, 1/4W
R5,R6	RCR07G200J		Res, 20 +/-5%, 1/4W
R7,R12	RN55C1002F		Res, 10K +/-1%, 1/10W
R8	RN55C9093F		Res, 909K +/-1%, 1/10W
R9	RN55C5111F		Res, 5.11K +/-1%, 1/10W
R10	RN55C9092F		Res, 90.9K +/-1%, 1/10W
R13,R14	RN55C2211F		Res, 2.21 +/-1%, 1/10W
R23	RCR07G511J		Res, 510 +/-5%, 1/4W
RN1	104796	23207	Resistor Network
CR1	104403-G6	23207	Diode
Y1	107540	23207	Crystal, 1.8432 MHz
U1,U38,U44	104220-G4	23207	IC, Quad 2-Input OR Gate
U2,U3,U13,U15	104331	23207	IC, Hex Tri-state Buffer
U5,U6,U12 U14,U19,U20,U41	104216-G3	23207	IC, Hex Tri-state Buffer
U7	104319	23207	IC, Micro Processor

REPLACEABLE PARTS LIST (Cont'd)

626-PA-6012

PC Board, Communications Module P/N 110532

REF DESIG	PART NO.	MAN CODE NO.	DESCRIPTION
U8,U9	104221-G1	23207	IC, 3 to 8 Decoder
U10,U16	104220-G2	23207	IC, Hex Inverter
U11	104221-G8	23207	IC, Quad 2-Input NOR Gate
U17	104234-G1	23207	IC, CMOS 1K x 4 RAM
U18	104214-G2	23207	IC, Quad 2-Input AND Gate
U21	104220-G5	23207	IC, Dual D Flip Flop
U22	104221-G7	23207	IC, Dual 2 to 4 Decoder
U24	104249-G1	23207	IC, ACIA
U25	104317	23207	IC, Serial Interface
U26	104222-G2	23207	IC, Line Receiver
U27	104222-G1	23207	IC, Line Driver
U29-U36	104235	23207	IC, CMOS 2K x 8 RAM
U37,U42,U43	104202-G3	23207	IC, Quad D Latch
U39	104201-G1	23207	IC, Dual D Flip Flop
U40	104238-G2	23207	IC, Dialer Chip
U45	104236-G1	23207	IC, Op Amp
U47	104390-G1	23207	IC, Octal Transceiver
XU17	104930	23207	IC Socket, 18 pin
XU23,XU25, XU28-XU36	104933	23207	IC Socket, 24 pin
XU24	104934	23207	IC Socket, 28 pin
XU7	104935	23207	IC Socket, 40 pin

REPLACEABLE PARTS LIST (Cont'd)

626-PA-6012

PC Board, Communications Module P/N 110532

REF DESIG	PART NO.	MAN CODE NO.	DESCRIPTION
J3,J5	107486-G2	23207	Header Assy, 10 pos
J4	87227-8	00779	Header Assy, 16 pos

REPLACEABLE PARTS LIST

626-PA-6012

Main Assembly P/N 110532

REF DESIG	PART NO.	MAN CODE NO.	DESCRIPTION
	110526	23207	CPU/COMM Port Interface Cable Assembly
	110527	23207	Modem to CPU Interface Cable Assembly
	110540	23207	626/COMM Module Interface Cable Assembly
	110709	23207	Phone Line Cord
	110538	23207	OEM Modem Board
	110541	23207	Phone Jack PC Board Assy

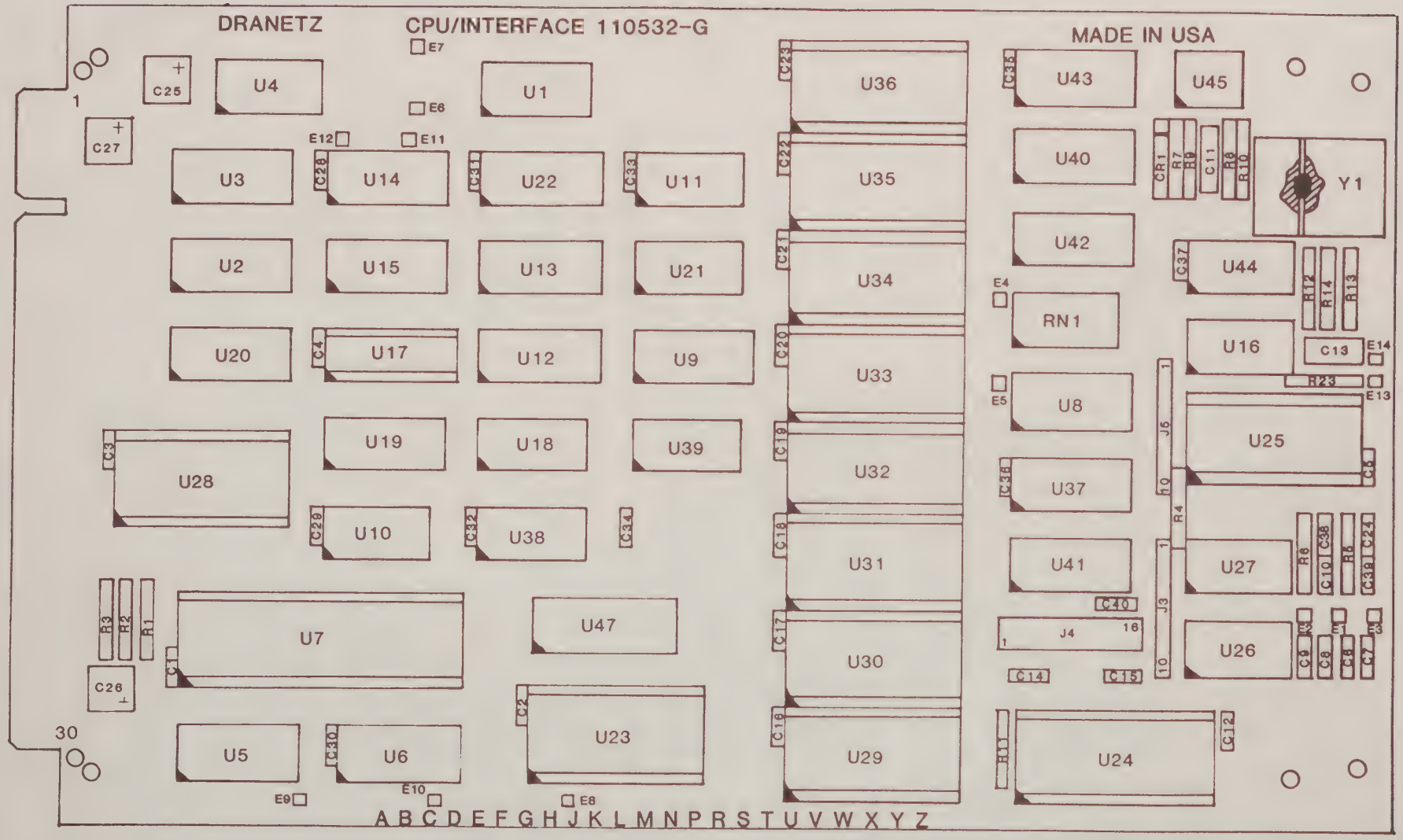

Figure 2. 6012 PC Board, Parts Location

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1000 NEW DURHAM ROAD, CN-91
EDISON, NEW JERSEY 08818

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(201) 287-3680
TWX: (710) 997-9553
CABLE: DRANETZ

NOTE: THIS COMPLETED FORM MUST ACCOMPANY RETURNED EQUIPMENT

CUSTOMER SHIPPING & BILLING INFORMATION

CUSTOMER P. O. • _____ P. O. DATE _____

SHIP TO: _____ INVOICE TO: _____

In Continental U. S., material will be returned by Dranetz to you by UPS, UPS Blue or other carrier chosen by Dranetz unless otherwise designated.

EQUIPMENT BEING RETURNED

Date of Original Purchase: _____ Original P. O. • _____

Model No. _____ S/N _____

Model No. _____ S/N _____

Ancillary equipment also being returned (If you neglect this, these items may not be returned to you)

- ☐ Power & Other Cables _____
- ☐ Instr. Book _____
- ☐ Plug-ins (incl. S/N) _____
- ☐ Connectors _____
- ☐ Other _____

RETURN AUTHORIZATION

Have you discussed the problem with Dranetz Sales or Service personnel?

Dranetz Return Authorization • _____

By _____

If so, with whom _____ Date: _____

Whom should the Dranetz Customer Service Dept contact for technical questions?

( )

NAME (Print) DEPARTMENT TELEPHONE

DESCRIPTION OF PROBLEM

Please be detailed, explicit and complete. Include test data, if this helps to describe the problem.
IMPORTANT: Repairs cannot be made unless this section is completely filled out.
(Attach added sheets if necessary)

CHECK WHERE APPLICABLE: IS MALFUNCTION RELATED TO: Warmup ☐ Temperature ☐
Intermittency ☐ Mechanical Handling ☐ Visual Defects ☐ Grounding ☐ Test Data Attached ☐

INITIATOR OF THIS ORDER

NAME/TITLE SIGNATURE TELEPHONE

(SEE OTHER SIDE FOR INSTRUCTIONS)

IMPORTANT (ENCLOSE THIS ENTIRE FORM WITH EQUIPMENT)

INSTRUCTIONS FOR REPAIR ORDER - DRANETZ TECHNOLOGIES

IMPORTANT: FOLLOW INSTRUCTIONS & USE THIS FORM. IT IS DESIGNED TO HELP US HELP YOU.

1. Before returning equipment to our factory, call our Customer Service Department, Tel:(201) 287-2535 Give the model No., serial number, and information on the problem.

   A. Our specialists may be able to solve your problem rapidly without equipment return.

   B. If equipment return is needed, you will be supplied with appropriate instructions and authorization information to expedite service.

2. If return is to be made,

   A. Fill out the other side of this form COMPLETELY.

   B. Enclose original of form INSIDE the shipping carton, preferably attached by masking tape to the equipment.

   C. Ship prepaid (including insurance); we will return prepaid unless otherwise advised by you.

   D. IMPORTANT - PACK PROPERLY! SHIPPING DAMAGE WILL BE CHARGED TO YOU!

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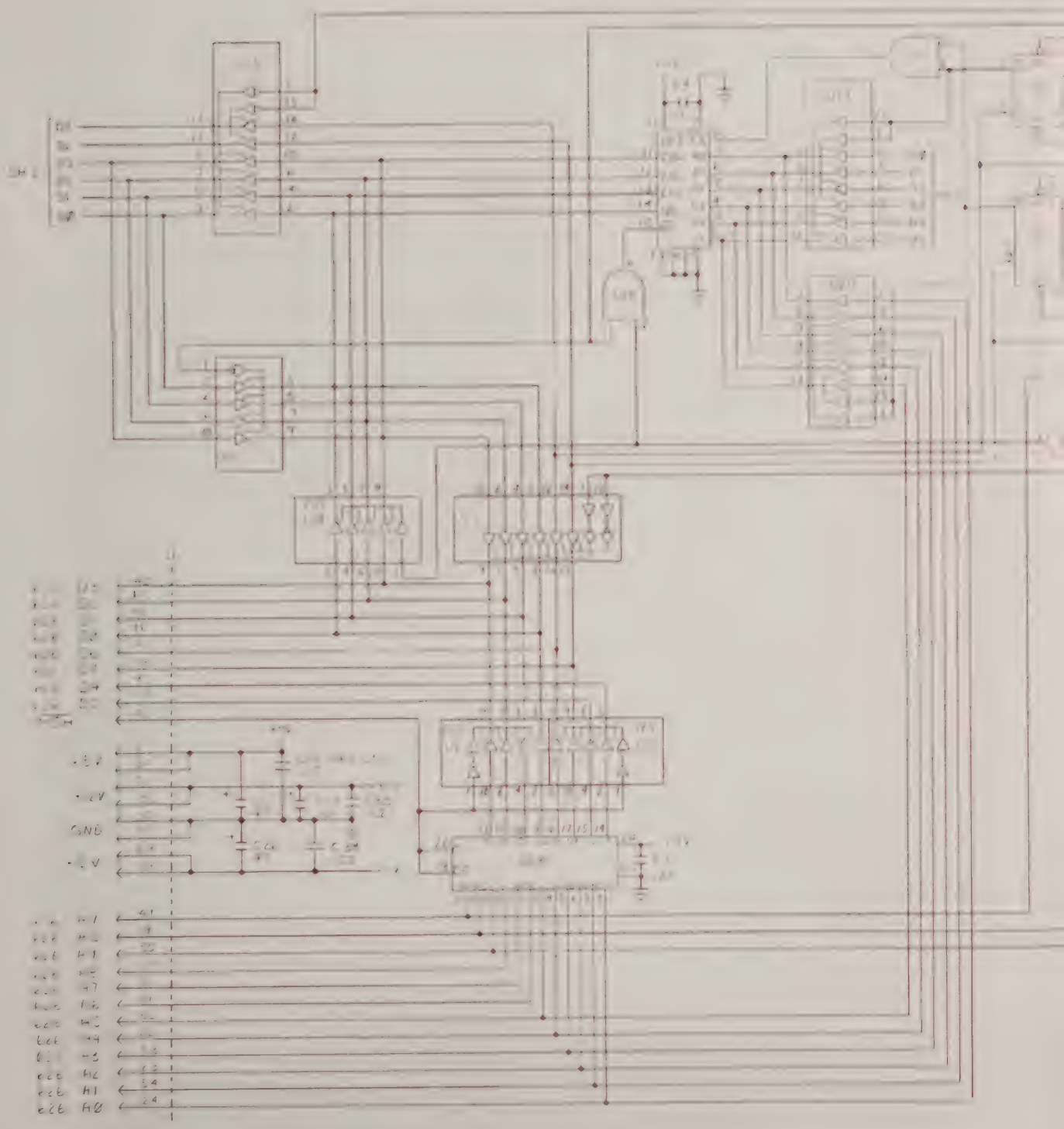
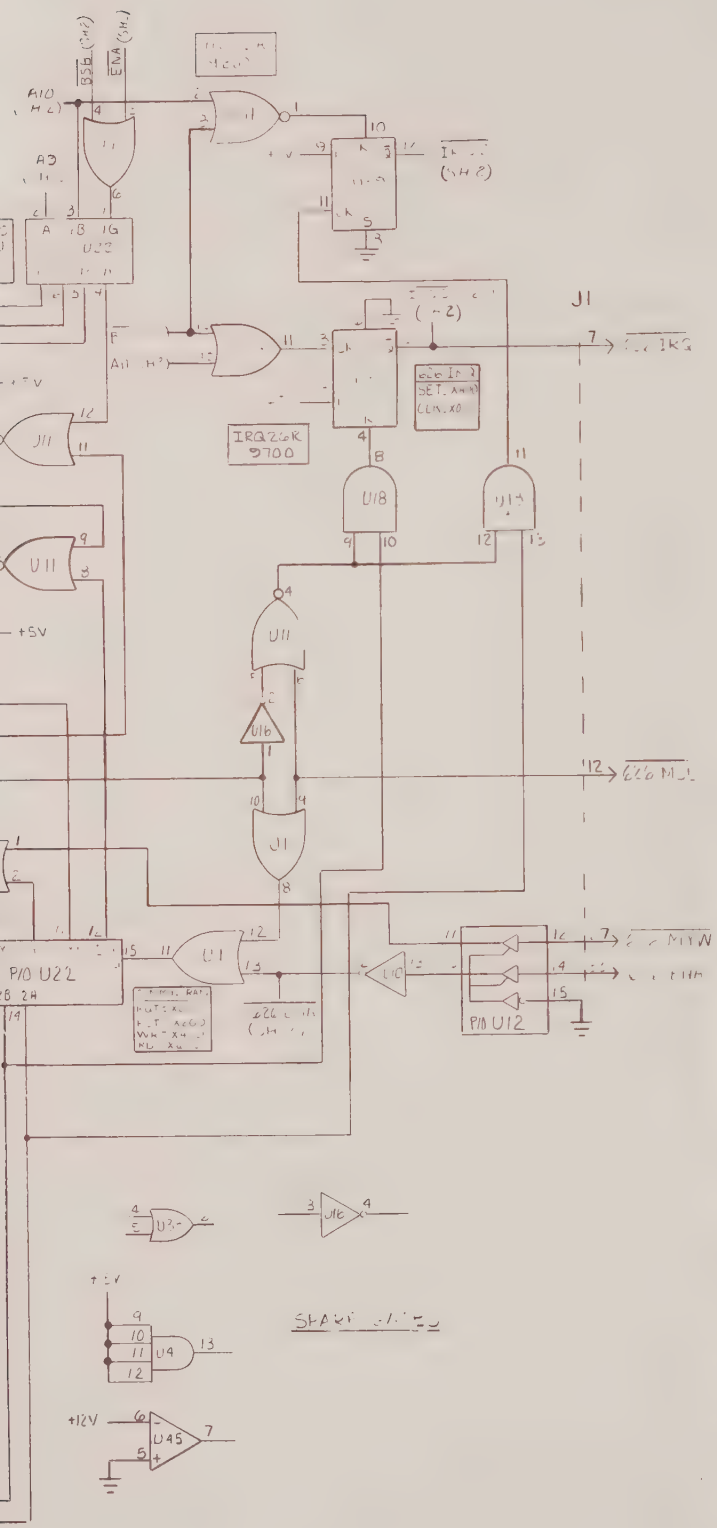
FILL OUT OPPOSITE SIDE OF THIS FORM AND RETURN WITH EQUIPMENT.





NOTES
UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE [illegible] MICROFARADS.
RESISTOR VALUES ARE IN OHMS, 1/4 W, ±5%.
2 (J) DENOTES [illegible]
3 -G1 VERSION [illegible]
-G2 VERSION [illegible]

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	[illegible]	8	[illegible]			
[illegible]	[illegible]	[illegible]	[illegible]			
[illegible]	[illegible]	[illegible]	16			
[illegible]	[illegible]	1,21	8			
U9	[illegible]	8	16			
U10,16	3N74[illegible]	7	14			
U11	CD4001UFF		14			
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[illegible]	[illegible]	[illegible]				24
[illegible]	[illegible]	[illegible]	16			
[illegible]	[illegible]	7	14			
[illegible]	MC1440[illegible]	5	16			
[illegible]	[illegible]			8	4	
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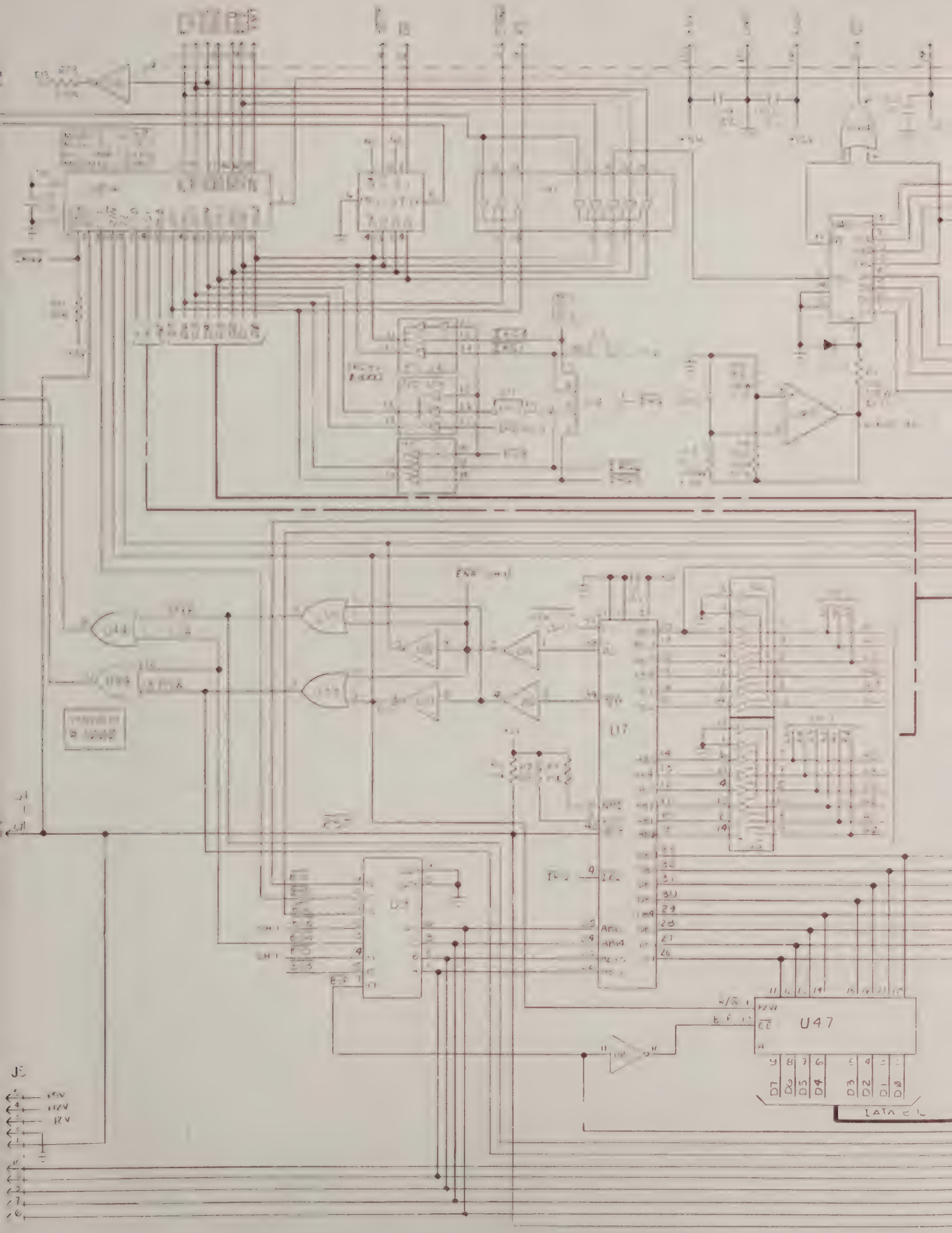
[illegible]		5				16

Figure 3. 626-PA-6012 (110537-G1), Schematic Diagram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U47
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D6
D5
D4
D3
D2
D1
D0
+5V
+12V
-12V

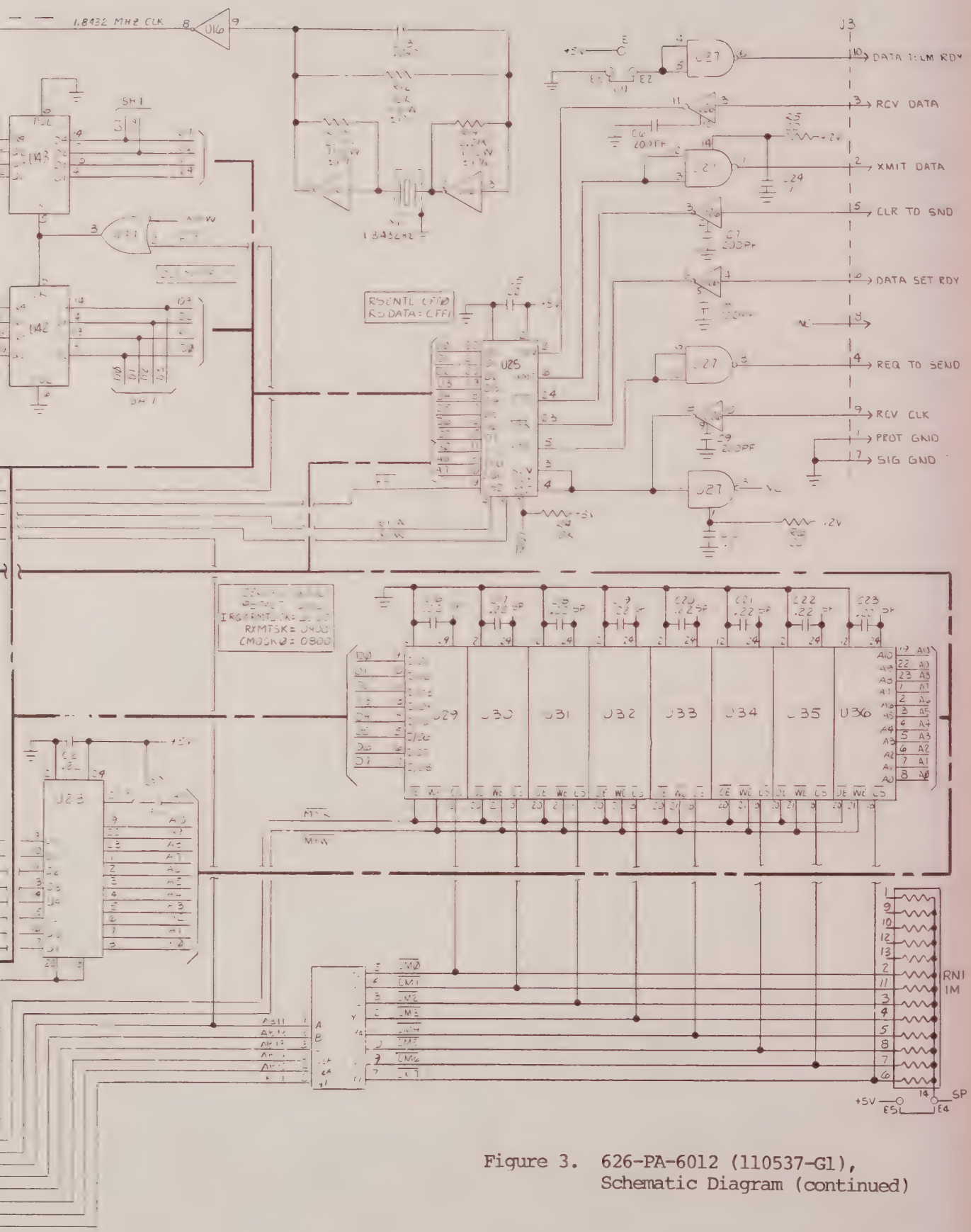

Figure 3. 626-PA-6012 (110537-G1), Schematic Diagram (continued)

LAST ONE!

Customer gets a copy

Return this to the floor

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